IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	Before the Board of Appeals
Teruaki Uehara	:	Appeal No.:
Serial No.: 10/642,735	:	Group No.: 2193
Filed: August 19, 2003	:	Examiner: C. Ngo
	:	Conf. No. 3778

For: ARITHMETIC UNIT AND METHOD FOR DATA STORAGE AND READING

September 11, 2008

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For: ARITHMETIC UNIT AND METHOD FOR DATA STORAGE AND READING

APPEAL BRIEF

U.S. Patent and Trademark Office
****via electronic filing****
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Date: September 11, 2008

Sir:

In response to the Final Office Action dated February 13, 2008, and further responsive to the Notice Of Appeal filed on June 11, 2008, this corresponding Appeal Brief is respectfully submitted.

I. REAL PARTY IN INTEREST

This application is assigned to Oki Electric Industry Co., Ltd., which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that may be related to, that would directly affect or be directly affected by, or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claims 1, 3, 5, 6 and 21-25 (rejected).

Claims 2, 4 and 7-20 (canceled).

Claims 1, 3, 5, 6 and 21-25 have been finally rejected. Accordingly, the rejections of claims 1, 3, 5, 6 and 21-25 are being appealed.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action dated February 13, 2008. Thus, the claims have not been amended subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to an arithmetic unit for executing an arithmetic process with respect to data in which a word is not standard 2^n-bit wide.[1]

The arithmetic unit as broadly featured in independent claim 1 includes in combination a memory for storing data (17 in Fig. 1); an arithmetic logic unit (13' in Fig. 1) for executing a predetermined arithmetic operation (e.g., page 26, line 24 to page 29, line 1) with respect to the data from the memory (17) to provide first output data, the data being grouped into one of several patterns (e.g., Fig. 13); a register (27 in Fig. 1) for temporarily storing the data read from the memory (17), and providing the temporarily stored data as second output data (e.g., page 5, lines 14-15); and a combining circuit (29 in Fig. 1) for receiving the first output data from the arithmetic logic unit (13') and the second output data from the register (27), and outputting combined data which is provided by replacing a part of the second output data with a part of the first output data based on the pattern of the data from the memory (17) (e.g., page 24, lines 10-15; page 25, lines 14-19; and page 26, lines 16-21), wherein when the part of the second output data is replaced with the part of the first output data, the combining circuit (29) shifts a position of data to be replaced in the

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1 In the description to follow, citations to various reference numerals, figures and corresponding text in the specification are provided solely to comply with Patent Office rules. It should be understood that these reference numerals, figures, and text are exemplary in nature, and not in any way limiting of the true scope of the claims. It would therefore be improper to import anything into any of the claims simply on the basis of **exemplary** language that is provided here only under the obligation to satisfy Patent Office rules for maintaining an Appeal.

second output data by a predetermined number of bits every time an operation process is executed (e.g., page 17, lines 4-7; page 19, lines 5-8; page 21, lines 6-9; and page 30, lines 13-17).

As broadly featured in independent claim 21, the arithmetic unit includes in combination a memory (17 in Fig. 1) storing data; an arithmetic logic unit (13' in Fig. 1) executing a predetermined arithmetic operation (e.g., page 26, line 24 to page 29, line 1) with respect to the data from the memory (17) to provide first output data, the data being grouped into one of several patterns (e.g., Fig. 13); a register (27 in Fig. 1) temporarily storing the data read from the memory (17), and providing the temporarily stored data as second output data (e.g., page 5, lines 14-15); and a combining circuit (29 in Fig. 1) that carries out an operation process by receiving the first output data from the arithmetic logic unit (13') and the second output data from the register (27), replacing a part of the second output data from the register (27) with a part of the first output data from the arithmetic logic unit (13') based on the pattern of the data from the memory (17) to provide combined data (e.g., page 24, lines 10-15; page 25, lines 14-19; and page 26, lines 16-21), and outputting the combined data to the memory (17) for storage.

As broadly featured in dependent claim 24, the arithmetic unit further includes a shifter (11 in Fig. 1) for shifting data received from the memory (17) and outputting the shifted data to the arithmetic logic unit (13') (e.g., page 15, lines 4-6).

As broadly featured in dependent claim 25, the arithmetic unit further includes in

combination an accumulator (15 in Fig. 1) for temporary storing data output from the arithmetic logic unit (13') (e.g., page 18, lines 5-7).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues on Appeal are:

(1) The rejection of claims 1, 3, 5, 6 and 21-25 under 35 U.S.C. 101 as being directed to non-statutory subject matter;

(2) The rejection of claims 21 and 23 under 35 U.S.C. 102(b) as being clearly anticipated by the Getzlaff et al. reference (U.S. Patent No. 5,754,875); and

(3) The rejection of claims 24 and 25 under 35 U.S.C. 103(a) as being unpatentable over the Getzlaff et al. reference.

VII. ARGUMENTS

(1) Claims 1, 3, 5, 6 and 21-25 are directed to statutory subject matter in compliance with 35 U.S.C. 101

Claims 1, 3, 5, 6 and 21-25 have been rejected under 35 U.S.C. 101 as allegedly being directed to non-statutory subject matter. This rejection is respectfully traversed for at least the following reasons.

Claims 1, 3, 5 and 6

The Examiner has apparently asserted that all the claims are directed to an

apparatus for merely performing manipulations and calculations of data, and that in order for such a claimed invention to be statutory, the claimed invention must accomplish a practical application and not be directed to a preemption of a calculation and/or manipulation of data. The Examiner has asserted that the claimed invention in this case must transform an article or physical object to a different state or thing, or produce a useful, concrete and tangible result, and not cover every substantial practical application (see page 2, lines 4-10 of the Final Office Action). The Examiner has relied upon the Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility, 1300 OG 142, 22 November 2005, which is summarized in Manual of Patent Examining Procedure (MPEP) section 2106.

As explained in the Interim Guidelines, the first step in determining whether a claim recites patent eligible subject matter is to determine whether the claim falls within one of the four statutory categories of invention recited in 35 U.S.C. 101: process, machine, manufacture and composition of matter. The latter three categories define "things" or "products", while a "process" consists of a series of steps or acts to be performed.

In order for a process to comply with 35 U.S.C. 101, the process must (1) be tied to another statutory class (such as a particular apparatus), **or** (2) transform underlying subject matter (such as an article or materials) to a different state or thing. If **neither** of these requirements is met by the claim, the method is not a patent eligible process under 35 U.S.C. 101. That is, if the process is either tied to another statutory class, or

on the other hand transforms underlying subject matter, 35 U.S.C. 101 is satisfied.

An example of a method claim that would **not** qualify as a statutory process would be a claim that recited purely mental steps. Thus, to qualify as a statutory process under 35 U.S.C. 101, the claims should positively recite the other statutory class (the thing or product) to which it is tied, for example by identifying the apparatus that accomplishes the method steps, **or** positively recite the subject matter that is being transformed, for example by identifying the material that is being changed to a different state.

Accordingly, the first step in determining whether a claim is directed to statutory subject matter under 35 U.S.C. 101 is to identify whether the claim falls within one of the four enumerated categories of patentable subject matter recited in section 101 (process, machine, manufacture or composition of matter).

If the claim **does not fall** within one of the four enumerated categories of patentable subject matter, the analysis proceeds to consideration of ***Judicial Exceptions***, followed by ***Practical Application***, and then ***Preemption***. On the other hand, if the claim **does fall** within one of the four enumerated categories of patentable subject matter, **the claim is deemed as directed to statutory subject matter in compliance with 35 U.S.C. 101, and the analysis is thus concluded** (see MPEP section 2106 IV.B.).

The arithmetic unit of claim 1 includes in combination among other features a memory for storing data; an arithmetic logic unit "for executing a predetermined

arithmetic operation with respect to the data from the memory to provide the first output data, the data being grouped into one of several patterns"; a register for temporarily storing data; and a combining circuit that replaces a part of second output data with a part of first output data.

Since the arithmetic unit of claim 1 features the above noted physical components, the apparatus of claim 1 as a whole is more than merely an abstract idea (mathematical algorithm), natural phenomena, or a law of nature. That is, a claim that is merely an abstract idea, natural phenomena, and a law of nature would not include physical components such as a memory, an arithmetic logic unit, a register and a combining circuit as featured in claim 1. The arithmetic unit of claim 1 is not a literary work, is not rules to play a game, is not a legal agreement, is not a signal per se, and is not a computer program, which all fall outside one of the enumerated categories under section 101. Claim 1 is clearly directed to a machine (apparatus), and falls within one of the four enumerated categories of patentable subject matter recited in 35 U.S.C. 101. The arithmetic unit of claim 1 is thus directed to eligible subject matter under 35 U.S.C. 101.

The requirement on page 2 of the Final Office Action dated February 13, 2008, that the claims must accomplish a practical application, or produce a useful, concrete and tangible result, is thus incorrect and irrelevant, because claim 1 clearly falls within one of the four statutory categories of eligible subject matter under 35 U.S.C. 101. That is, these requirements would apply as considered with respect to the ***Practical***

Application step as described in the Interim Guidelines as noted above. However, since claim 1 clearly falls within one of the four enumerated categories of patentable subject matter, consideration of the ***Practical Application*** step of the test is unnecessary.

In the last sentence on page 2 of the Final office Action, the Examiner has asserted that the claims cover "every substantial practical application" and preempt the claimed manipulation and calculation of data. However, the arithmetic unit of claim 1 expressly features in combination a memory, an arithmetic logic unit, a register and a combining circuit that function in a clearly recited and interrelated manner. The arithmetic unit of claim 1 thus does not cover "every substantial practical application" and does not preempt. In contrast, claim 1 covers an arithmetic unit including the recited components that function in the recited manner. It would appear that the Examiner has impermissibly disregarded the above noted features of claim 1 to maintain this rejection.

Accordingly, Appellant respectfully submits that the arithmetic unit of claim 1 is directed to statutory subject matter, and that claims 1, 3, 5 and 6 are thus in compliance with 35 U.S.C. 101. Appellant therefore respectfully requests that this rejection of claims 1, 3, 5 and 6 be withdrawn for at least these reasons.

Claims 21-25

The arithmetic unit of claim 21 includes in combination among other features a

memory storing data; an arithmetic logic unit "executing a predetermined arithmetic operation with respect to the data from the memory to provide first output data, the data being grouped into one of several patterns"; a register "temporarily storing the data read from the memory, and providing the temporarily stored data as second output data"; and a combining circuit "that carries out an operation process by receiving the first output data from the arithmetic logic unit and the second output data from the register, replacing a part of the second output data from the register with a part of the first output data from the arithmetic logic unit based on the pattern of the data from the memory to provide combined data, and outputting the combined data to the memory for storage".

Appellant respectfully submits that the arithmetic unit of claim 21 is statutory under 35 U.S.C. 101 for at least somewhat similar reasons as set forth above with respect to claim 1. That is, since the arithmetic unit of claim 21 includes in combination a memory, an arithmetic logic unit, a register and a combining circuit as physical components, the arithmetic unit of claim 21 clearly is directed to a machine (apparatus) and thus falls within one of the four enumerated categories of patentable subject matter recited in 35 U.S.C. 101. Moreover, the arithmetic unit of claim 21 as including the above noted physical components in combination does not cover "every substantial practical application", and does not preempt, as further asserted by the Examiner. Accordingly, Appellant respectfully submits that the arithmetic unit of claim 21 is directed to statutory subject matter, and that claims 21-25 are thus in compliance with 35 U.S.C. 101. Appellant therefore respectfully submits that this rejection of claims 21-

25 under 35 U.S.C. 101 be withdrawn for at least these reasons.

(2) Claims 21 and 23 distinguish over the Getzlaff et al. reference

Claims 21 and 23 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Getzlaff et al. reference. This rejection is respectfully traversed for the following reasons.

Claims 21 and 23

The Examiner has characterized the node after ALU (arithmetic and logic unit) 10 in Fig. 2 of the Getzlaff et al. reference as the combining circuit of the claims (see page 3 of the Final Office Action dated February 13, 2008). The node after ALU 10 in Fig. 2 of the Getzlaff et al. reference has input thereto data lines 282, 283 and 17 each having 32-bit width, and has output therefrom data line 285 having 64-bit width.

However, Appellant respectfully submits that the node after ALU 10 in Fig. 2 of the Getzlaff et al. reference does not carry out an operation process by receiving a first output data from an arithmetic logic unit and a second output data from a register, does not replace a part of the received second output data from a register with a part of the received first output data from an arithmetic logic unit based on a pattern of the data from a memory to provide combined data, and does not output the combined data to memory for storage, as would be necessary to meet the features of claim 21.

As described in column 4, lines 14-20 of the Getzlaff et al. reference with respect to Fig. 2:

"The two data words stored in the ORA (12) and the ORB (13) are then transmitted to the ALU (10) to be processed, e.g. to be added. The result of this addition has 32 bits and is output on data line (17). This resultant data word can be ***combined*** *with another 32 bit data word coming from the ORA (12)* ***or*** *the ORB (13)" (*our emphasis added*)."*

As further described in column 4, lines 27-31 of the Getzlaff et al. reference with respect to Fig. 2:

"In this manner, the resultant data word outputted by the ALU (10) can be ***combined*** *with a data word which is outputted by the ORA (12)* ***or*** *the ORB (13) in the same cycle and which bypasses the ALU (10) via the data lines (282, 283."* (our emphasis added).

As still further described in paragraph 4, lines 51-56 of the Getzlaff et al. reference with respect to Fig. 2, both the data words in ORB 12 and ORB 13 may bypass ALU 10 via data lines 282 and 283 respectively, so that the bypassing data words are combined and then presented as a 64-bit data word on data line 285.

Accordingly, it should be readily clear that the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference merely **combines** two 32-bit data words provided thereto on any two of data lines 282, 283 and 17, to provide a 64-bit data word to data bus 230 via line 285. That is, the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference merely **combines** whatever data words are provided thereto. For example, the node subsequent ALU 10 combines a 32-bit word from ALU 10 with one 32-bit word

that happens to be provided from either of ORA 14 or ORA 15. As a further example, the node subsequent ALU 10 combines one 32-bit word from ORA 12 with one 32-bit word from ORB 13 when provided thereto when ALU 10 is bypassed. The node subsequent ALU 10 does not **replace** a part of received data. Particularly, in absence of any further specific description in the Getzlaff et al. reference, and in view of the fact that data lines 282, 283 and 17 are merely tied to line 285, it can only reasonably be presumed that the 64-bit data word as provided on data line 285 from the node subsequent ALU 10 consists merely of one 32-bit data word appended to or somehow combined with another 32-bit data word. The manner in which the words are combined are not otherwise described in detail in the Getzlaff et al. reference.

Appellant respectfully submits that the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference is not described or even remotely suggested as receiving first output data (from ALU 10) and second output data (from ORA 12 **or** ORB 13), and manipulating the received data by **replacing** a part of the received second output data (from ORA 12 **or** ORB 13) with a part of the received first output data (from ALU 10). Partitioning of received output data, and replacement of a part of this partitioned data with a part of other partitioned received output data is not disclosed in the Getzlaff et al. reference as relied upon.

Moreover, even assuming for the sake of argument that the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference could somehow be interpreted as replacing a part of received second output data from a register with a part of received

first output data from an arithmetic logic unit (which Appellant does not concede), the Getzlaff et al. reference does not disclose or even remotely suggest that any such combining or manipulation by the node subsequent ALU 10 is "based on the pattern of data from the memory", as would be necessary to meet the still further features of claim 21. The combining by the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference would appear in general to be based merely on which particular output data are provided on data lines 282, 283 and 17, not based on the pattern of data from a memory. The Getzlaff et al. reference as relied upon does not describe or address patterns of data.

In the Remarks section on page 4, lines 5-12 of the Final Office Action dated February 13, 2008, the Examiner has asserted that combining the output of ALU 10 in Fig. 2 of the Getzlaff et al. reference with the output from ORA 12 would be equivalent to replacing the output of ORB 13 with the output of ALU 10. However, as stated previously, the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference merely **combines** the data presented thereto, presumably be appending one data word to another. The node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference does not actively and specifically replace a part of a received output data with a part of another received output data. The Getzlaff et al. reference does not describe partitioning or replacement of received data by the node subsequent ALU 10.

The Getzlaff et al. reference as relied upon thus fails to meet the features of claim 21. Appellant therefore respectfully submits that the arithmetic unit of claim 21

distinguishes over the Getzlaff et al. reference as relied upon by the Examiner, and that this rejection of claims 21 and 23 is improper for at least these reasons.

(3) Claims 24 and 25 would not have been obvious in view of the Getzlaff et al. reference

Claims 24 and 25 have been rejected under 35 U.S.C. 103(a) as being clearly anticipated by the Getzlaff et al. reference. Appellant respectfully submits that the Getzlaff et al. reference as herein relied upon does not cure the above noted deficiencies of the Getzlaff et al. reference as set forth above with respect to claim 21. Accordingly, Appellant respectfully submits that claims 24 and 25 would not have been obvious in view of the Getzlaff et al. reference for at least these reasons.

Conclusion

Appellant respectfully submits that claims 1, 3, 5, 6, and 21-25 are directed to statutory subject matter in compliance with 35 U.S.C. 101.

Moreover, since claims 1, 3, 5 and 6 have not been rejected based upon prior art, Appellant respectfully submits that claims 1, 3, 5 and 6 should thus be allowed.

Appellant also respectfully submits that claims 21, 23, 24 and 25 distinguish over and would not have been obvious in view of the Getzlaff et al. reference, and should thus be allowed.

Moreover, since claim 22 has not been rejected based upon prior art, Appellant respectfully submits that claim 22 as dependent upon claim 21 includes allowable

subject matter.

Appellant therefore respectfully submits that the final rejection of claims 1, 3, 5, 6 and 21-25 should be withdrawn, and that these claims should be allowed, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

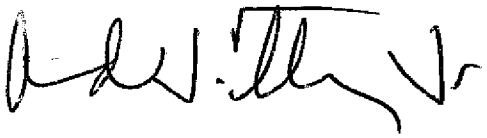
The required fee of $510.00 under 37 C.F.R. 41.20 for filing this Appeal Brief should be charged to Deposit Account No. 50-0238.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Appellant hereby petitions for an extension of one (1) month to September 11, 2008, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required under 37 C.F.R. 41.20 or 37 C.F.R. 1.17 and 1.136(a), or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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Appendix - Claims on Appeal

1. An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit for executing a predetermined arithmetic operation with respect to the data from the memory to provide first output data, the data being grouped into one of several patterns;

a register for temporarily storing the data read from the memory, and providing the temporarily stored data as second output data; and

a combining circuit for receiving the first output data from the arithmetic logic unit and the second output data from the register, and outputting combined data which is provided by replacing a part of the second output data with a part of the first output data based on the pattern of the data from the memory,

wherein when the part of the second output data is replaced with the part of the first output data, the combining circuit shifts a position of data to be replaced in the second output data by a predetermined number of bits every time an operation process is executed.

3. An arithmetic unit according to claim 1, wherein the memory includes a plurality of memory blocks.

5. An arithmetic unit according to claim 1, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

6. An arithmetic unit according to claim 1, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

21. An arithmetic unit comprising:

a memory storing data;

an arithmetic logic unit executing a predetermined arithmetic operation with respect to the data from the memory to provide first output data, the data being grouped into one of several patterns;

a register temporarily storing the data read from the memory, and providing the temporarily stored data as second output data; and

a combining circuit that carries out an operation process by receiving the first output data from the arithmetic logic unit and the second output data from the register, replacing a part of the second output data from the register with a part of the first output data from the arithmetic logic unit based on the pattern of the data from the memory to provide combined data, and outputting the combined data to the memory for storage.

22. An arithmetic unit according to claim 21, wherein the combining circuit shifts a position of data to be replaced in the second output data by a predetermined number of bits each successive operation process.

23. An arithmetic unit according to claim 21, wherein the memory includes a plurality of memory blocks.

24. An arithmetic unit according to claim 21, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

25. An arithmetic unit according to claim 21, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

Evidence Appendix

No evidence has been submitted under 37 C.F.R. 1.130, 1.131, or 1.132, or entered by the Examiner in connection with this pending Appeal.

Thus, there are **no** copies of evidence included in this Appendix.

Related Proceedings Appendix

There are no Appeals or Interferences that may be related to, directly affect, or be directly affected by or have a bearing on the Decision by the Board in this pending Appeal. Thus, there are **no** copies of decisions included in this Appendix.